

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A processor executing a plurality of instructions, comprising:
an arithmetic logic unit; and
a plurality of registers coupled to the ALU, each register programmable to store a register value;
wherein said processor executes a routine having a test and skip instruction that includes an immediate value and a reference to a register, the test and skip instruction performs a comparison using the immediate value and the register value stored in the referenced register, and selectively skips a subsequent instruction that follows the test and skip instruction based on the comparison;
wherein the subsequent instruction jumps to another routine.
2. (Original) The processor of claim 1 wherein the comparison is performed by comparing the immediate value to the register value in the referenced register.
3. (Previously presented) The processor of claim 2 wherein the processor skips the subsequent instruction if the immediate value does not match the register value and executes the subsequent if the immediate value does match the register value.
4. (Original) The processor of claim 1 wherein the comparison is performed by masking the register value in the referenced register with the immediate value and examining one or more bits in the masked version of the referenced register.

5. (Original) The processor of claim 4 wherein the masking is performed by ANDing the immediate value with the register value.
6. (Original) The processor of claim 1 wherein the instruction includes at least one bit that specifies how the comparison is to be performed.
7. (Original) The processor of claim 6 wherein the at least one bit specifies whether the register reference is to a register from a first group of registers or to a register from a second group of registers, and if a register from the first group of registers is specified by said bit, the comparison is performed by comparing the immediate value to the register value, and, if a register from the second group of registers is specified by said bit, the comparison is performed by masking the register value with the immediate value and examining one or more bits in the masked version of the referenced register.
8. (Original) The processor of claim 6 wherein the registers include a status register and if the register reference specified by said at least one bit is not the status register, the comparison is performed by comparing the immediate value to the register value in the referenced register, and, if the register reference specified by said at least one bit is the status register, the comparison is performed by masking the register value in the status register with the immediate value and examining one or more bits in the masked version of the status register.
9. (Previously presented) A method, of executing an instruction having a reference to a register, an immediate value, and a control bit that dictates one of at least two tests, the method comprising:
 - examining said control bit to determine its state;
 - if said control bit is in a first state, comparing the immediate value to the contents of the register referenced in the instruction and skipping a subsequent instruction based on the outcome of the comparison; or

if said control bit is in a second state, masking the contents of the register with the immediate value, testing one or more bits in the masked version of the contents of the register, and skipping a subsequent instruction based on the outcome of the testing.

10. (Original) The method of claim 9 wherein skipping the subsequent instruction comprises replacing the subsequent instruction with a no operation instruction.

11. (Previously presented) A system, comprising:
a main processor unit; and
a co-processor coupled to said main processor unit, wherein said co-processor selectively operates in a stack-based instruction mode and a register-based instruction mode,
wherein, during the register-based instruction mode, the co-processor executes an instruction that includes an immediate value and a reference to a register accessible to said co-processor, performs a comparison using the immediate value and the register value, and executes or skips a subsequent instruction based on the comparison.

12. (Original) The system of claim 11 wherein the co-processor performs the comparison by comparing the immediate value to the register value in the referenced register.

13. (Original) The system of claim 12 wherein the co-processor does not execute the subsequent instruction if the immediate value does not match the register value and executes the subsequent if the immediate value does match the register value.

14. (Original) The system of claim 11 wherein the co-processor performs the comparison by masking the register value in the referenced register with the immediate value and examining one or more bits in the masked version of the referenced register.

15. (Original) The system of claim 14 wherein the masking is performed by ANDing the immediate value with the register value.

16. (Original) The system of claim 11 wherein the instruction includes at least one bit that specifies how the comparison is to be performed.

17. (Original) The system of claim 16 wherein the bit specifies whether the register reference is to a register from a first group of registers or to a register from a second group of registers, and if a register from the first group of registers is specified by said bit, the comparison is performed by comparing the immediate value to the register value, and, if a register from the second group of registers is specified by said bit, the comparison is performed by masking the register value with the immediate value and examining one or more bits in the masked version of the referenced register.

18. (Original) The system of claim 11 further comprising wireless communication circuitry and said system comprises a cell phone.

19. (Currently amended) A programmable logic device comprising;
control logic; and
means for selectively changing an operating mode of the programmable logic device; and
a—means for decoding an instruction that includes an immediate value and a reference to a register for performing a comparison using the immediate value and a register value stored in the referenced register, and for causing

the processor to execute or not execute a subsequent instruction that follows the instruction based on the comparison;
wherein the subsequent instruction jumps to a routine associated with a particular operating mode.

20. (Original) The system of claim 19 including means for comparing the immediate value to the register value in the referenced register.